



Chelsio T7 ARM Unified Wire Solution for Linux

Release Notes



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I. Chelsio T7 ARM Unified Wire Solution

1. Introduction

This document provides details on Chelsio T7 ARM Unified Wire solution for Chelsio adapters in RC mode

 **Note** ***This feature is available for early access, having undergone a restricted validation cycle.***

2. New Features

The following new drivers have been added in this release:

- LIO iSCSI PDU Offload (Target) ARM driver.
- NVMe-oF iWARP (Target) ARM driver.
- NVMe-oF RoCEv2 (Target) ARM driver.
- NVMe-oF/TCP PDU Offload (Target) ARM driver.

3. Firmware Changelog

- Firmware has been updated from 2.1.25.0 to 2.1.26.0.
- Bug #46810: partial fix. mac, pcs, and phy changes for 1G link up
- Compile fixes to support any combination of RoCEV2=0 and MEMFREE_SENDFPATH=0
- Increased space for more firmware code.
- Accept (and ignore) RoCE settings even if the firmware is built without RoCEV2.
- Includes platform-level VPD fixes, updates the global cache configuration to check only the *init_done* bit instead of the idle state, and resolves link bringup failures caused by autonegotiation (AN) check issues.
- Fixed mc check in DUMP_OBQULP_TO_FW_BUF.
- Bug #46742: NVMe/TCP, iSCSI user mode: Fixed incorrect pointer returned by *ri_cqe()*.
- Bug #46810: Partial Fix: Corrected reset removal from Rx/Tx lanes of 1G PCS of port 2 and port 3. Setting correct SGMII speed mode(0x2) for 1G.
- Bug #46832 - Workaround: For 1G, SINKTXONLINKDOWN keeps dropping tx packets even after linkup. Therefore, a workaround has been added to avoid using SINKTXONLINKDOWN for 1G. SINKTX is used instead of SINKTXONLINKDOWN to drop the packets when link is down.
- Bug #44143:
 - Firmware support is added for S7410-BT adapter with Marvel PHY MV88X3540.
 - Moved phy fw flash functions to INIT region.
 - Removed T7 macro check from *t4fw_interface.h* since the file is used by drivers.
- Bug #46663: Fixed crash by enabling non-zero ntc_b if hashfilter is enabled.
- Bug #46898: T7C Prototype Chip Memory Update.
- Bug #46642 and #46888: Calculate and write out_th after writing mtu value because out_th depends on mtu value in T7.
- Bug #46893: Molex and Amphenol 10G DAC does not publish nominal rate exactly as 10.3G, some modules publish 10G and 12G. So corrected the module speed check accordingly.
- Bug #46810: WORKAROUND_PR46832: Link LED (LED0) is not linked to 1G LINK status register in rtl so it remains off for 1G link up. Workaround has been added in the firmware to manually turn on LED for 1G Link up..